Design & Verification Challenges for 3G/3.5G/4G Wireless Baseband MPSoCs

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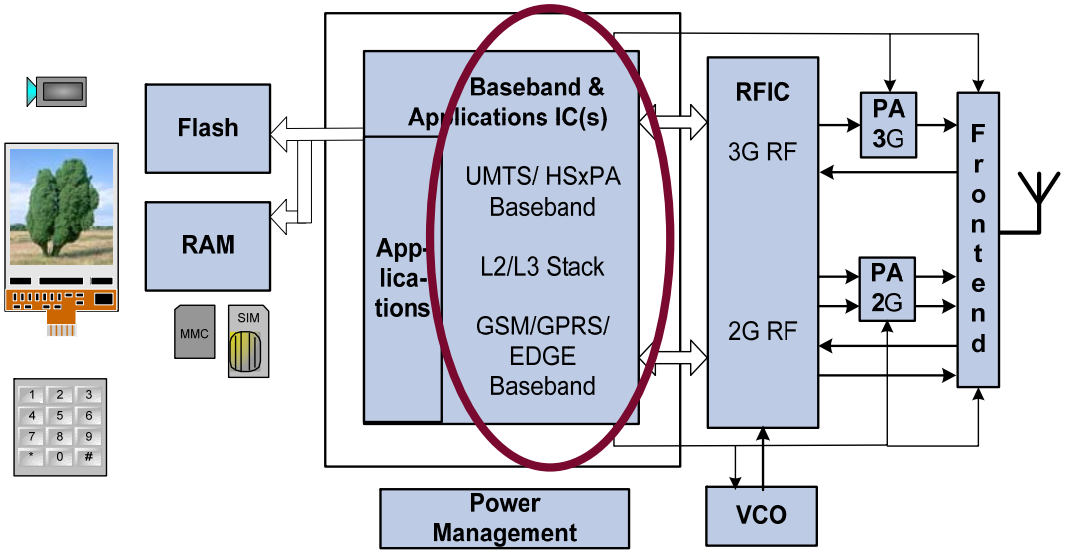
Never stop thinking

Outline

- challenges of 3G / 4G modem design
  - data throughput
  - latency
  - configurability
- wireless standards: a nightmare for system verification
- keys to success:
  - architecture
  - methodology
  - team-setup

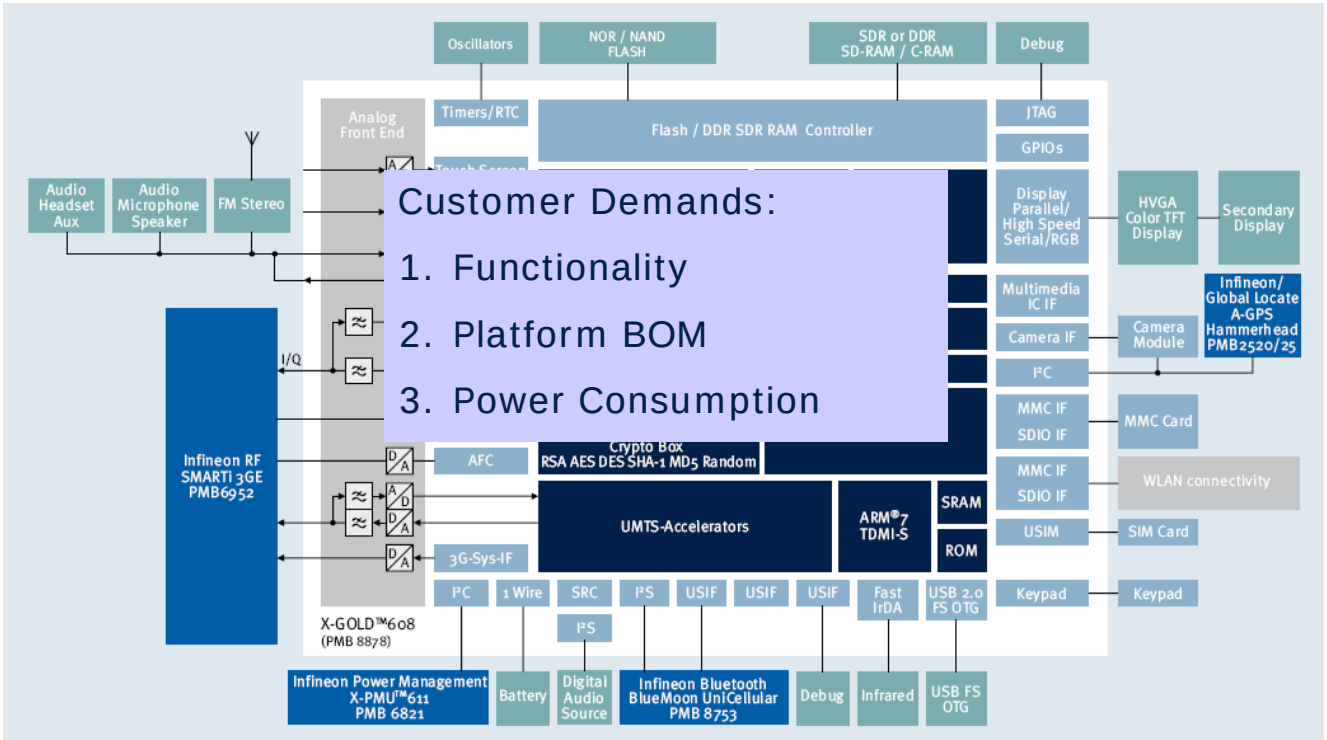
State of the Art Cellphone Platform

Focus: Digital Baseband



- A Heterogeneous Application Specific Multi-Processor SoC

Example: Infineon MP-EH Platform



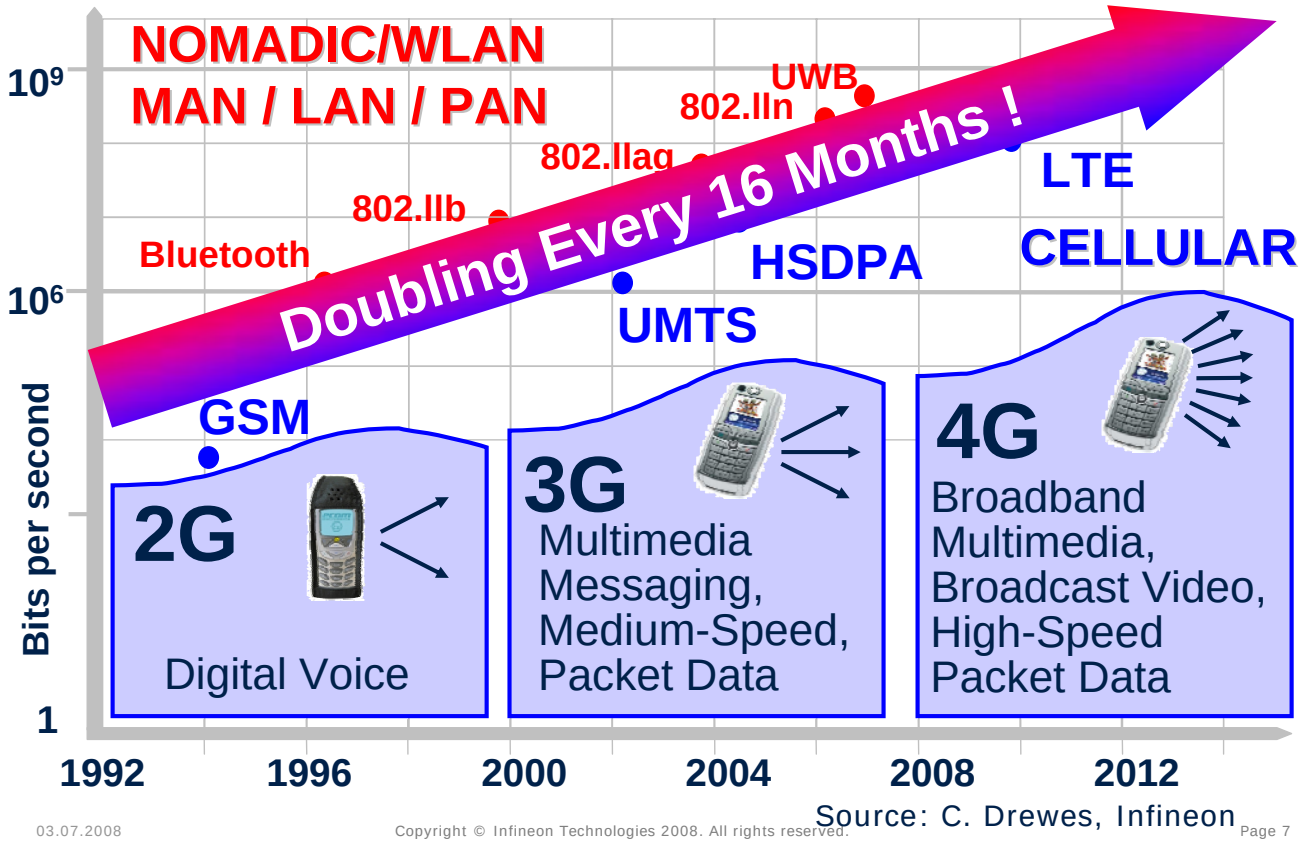
Why Dedicated Wireless MPSoCs?

- Thought Experiment: Modern digital cellular baseband
  - 20 GOPs peak signal processing demand (active)
  - 0 GOPs computational demand (standby, paging)
  - State of the art battery with 1400 mAh capacity
- What if we use 2 general purpose processors (like the ones in your desktop PC), assuming they would be powerful enough?
  - 60 W peak power consumption
  - 20 W standby power consumption
- Result
  - Active Time: 40 s
  - Standby Time: 30 min

- **We are building SoCs which are 100-1000x more energy efficient than state of the art GP processors and at the same time more efficient, faster, smaller and cheaper**

Throughput

Wireless Data Rate Evolution



Source: C. Drewes, Infineon

How to Address the Challenge

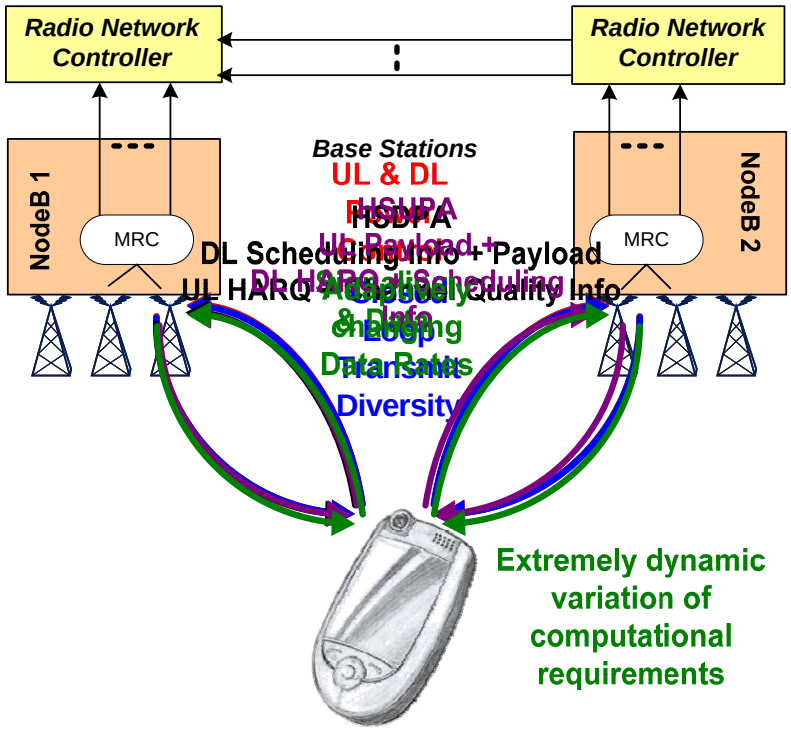
- "Shannon beats Moore"
  - Increasing gap between chip technology and throughput requirements
- Architecture + Algorithm
  - 2G: DSP Centric Architectures
  - 3.XG: + Dedicated HW Centric Architectures
  - 4G : + More Efficient Transmission Technology (OFDM)

Throughput requirements are extremely tough but can be met with state of the art architectures + methodology

Latency Requirements

Network <-> Modem Interaction

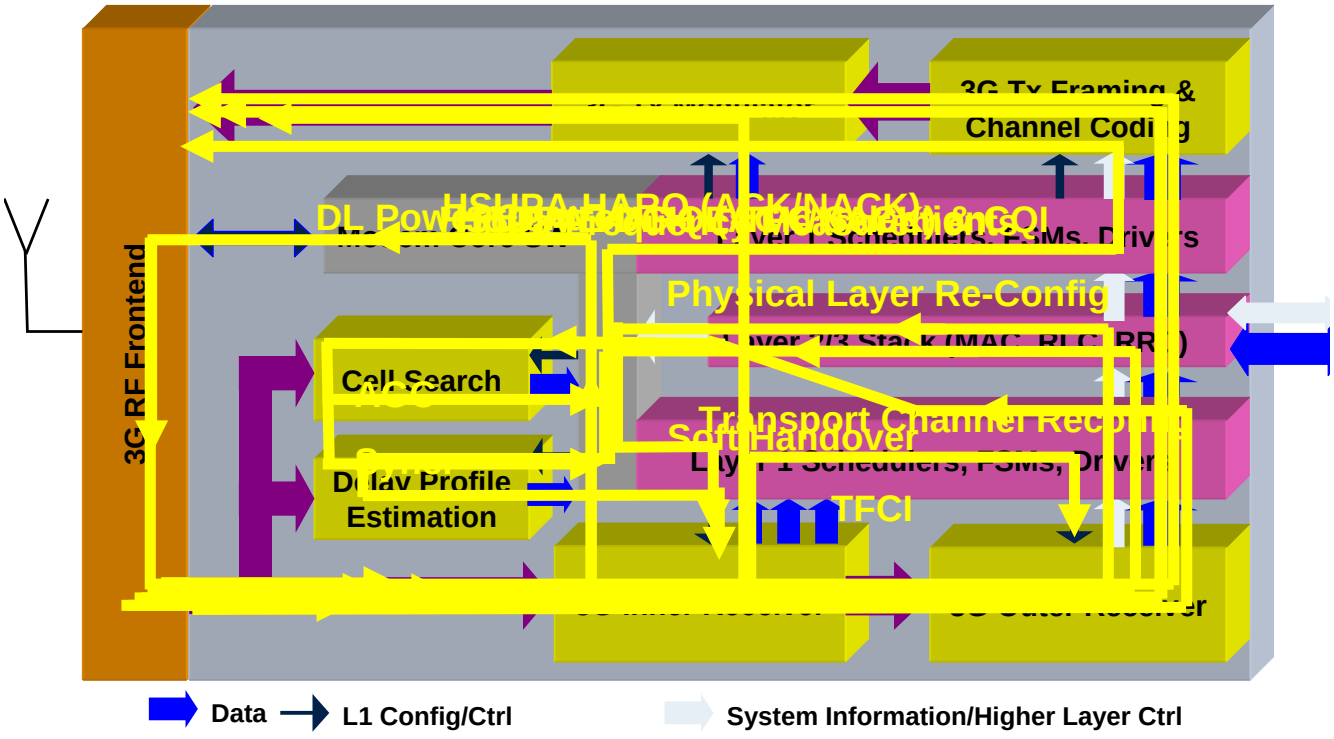
Network View



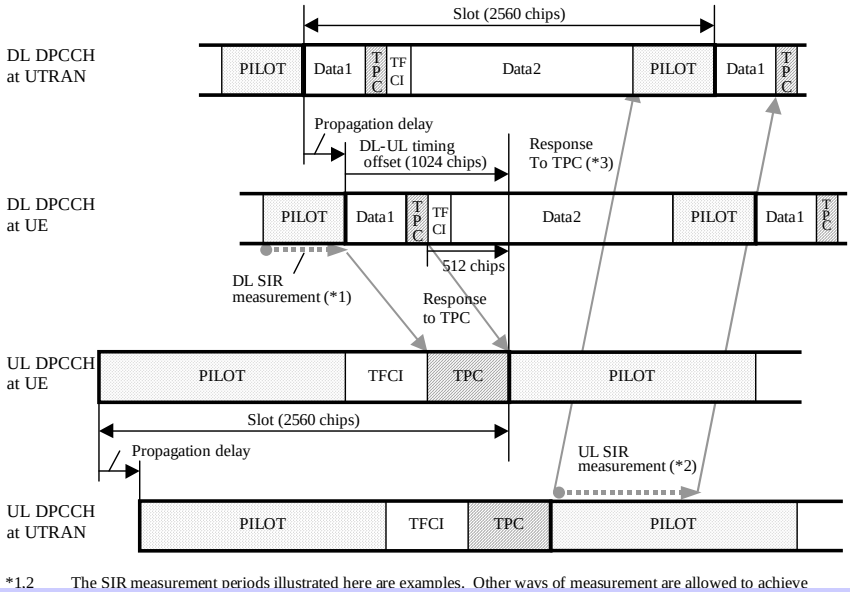
Highly advanced Signal Processing Algorithms plus Radio Link Adaptation and fast Scheduling

Network <-> Modem Interaction

Digital Baseband Architectural View



Example: 3G Power control

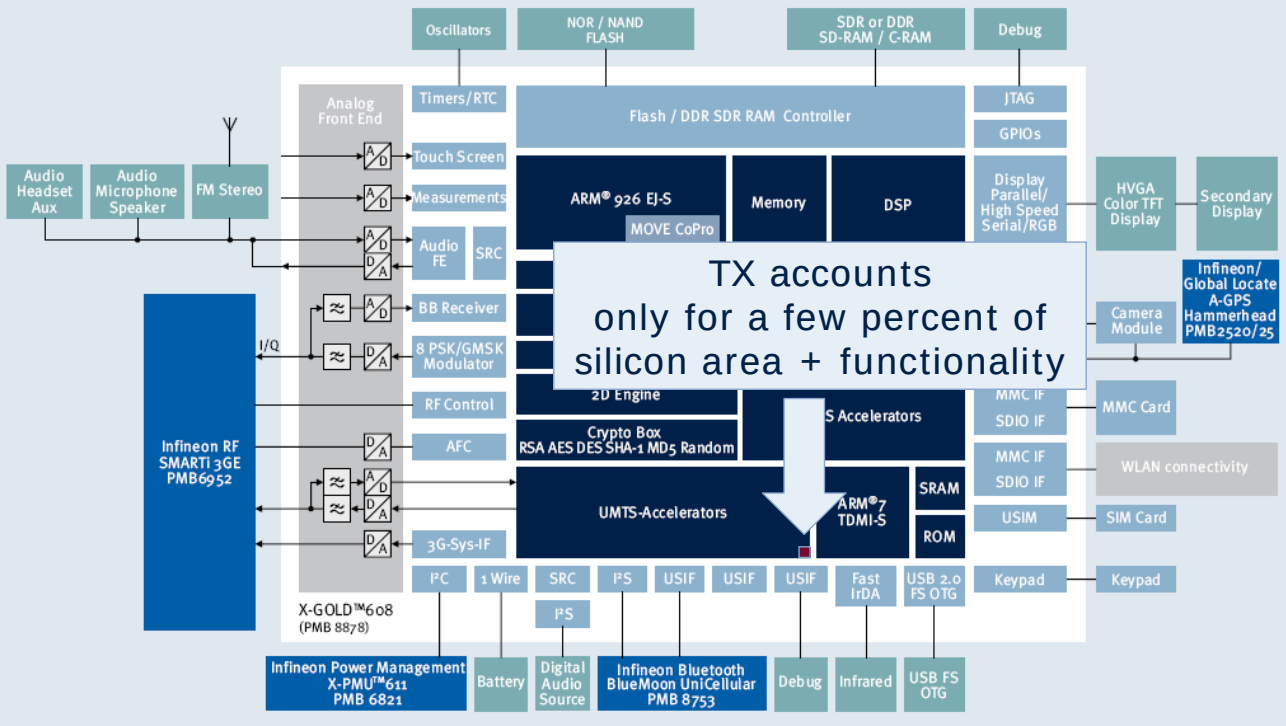


*1,2 The SIR measurement periods illustrated here are examples. Other ways of measurement are allowed to achieve

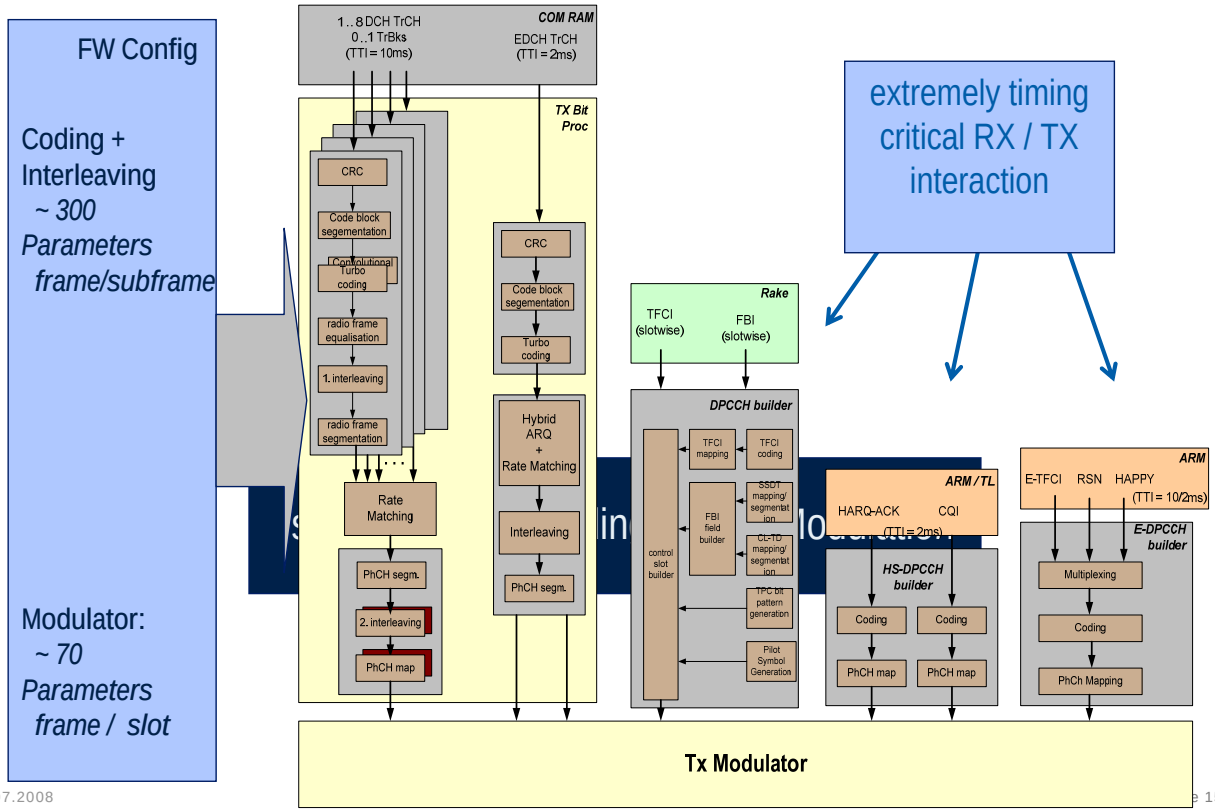
- Latency + Reconfiguration dominates system architecture
- Deterministic Scheduling is a *must*
- System Requirements must be known to the deepest detail

System Configurability

Example: UMTS TX



TX Processing for UMTS Rel. 6

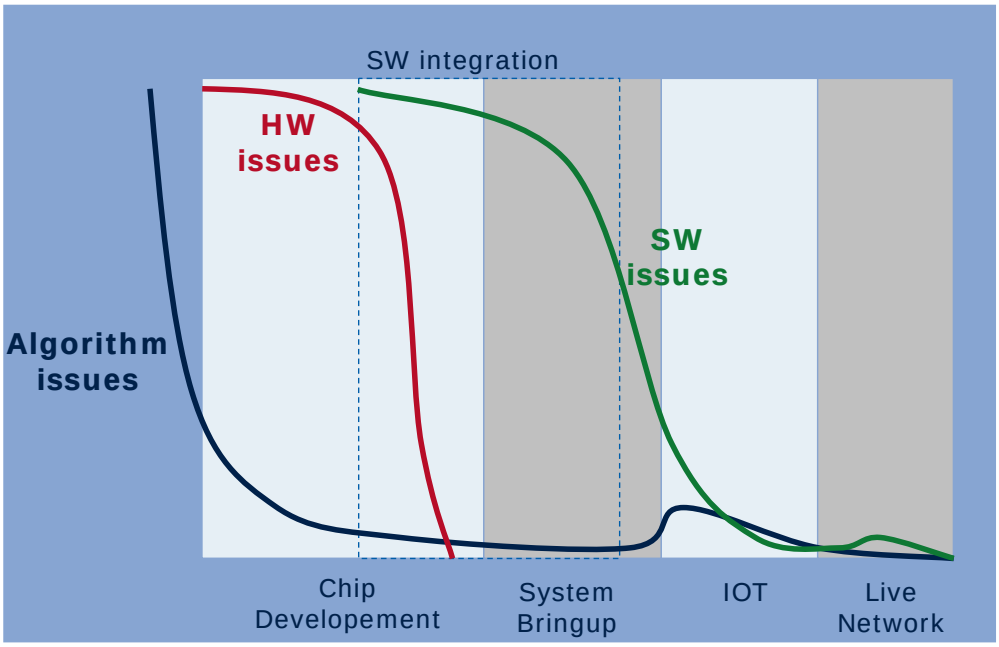


System Configurability

- 3G Transmitter:
  - Well defined serial bit processing
  - *But*: parameter flow can exceed data-flow
- 3G Receiver: ***much much*** more complicated
  - Multiple Base Stations, Soft Handover, Transmit Diversity
  - Multiple Rake Fingers, Receive Diversity
  - Complex Reconfigurations
  - Additional Neighbor Cell BCH

- No exhaustive test possible
- Even minimum testing leads to thousands of complex test-cases

System Development and Bringup



- Exhaustive verification impossible
- Flexibility required for *very* late changes

Architecture

System Design Paradigms

System Predictability

Static real-time scheduling based on Worst Case Execution Times (WCETs)

Localized Functionality

- Divide and Conquer: Cluster Functionality
  - → Self-Contained HW & FW Blocks
  - → Localized Functionality, Lean Interfaces
  - → Simplified Integration & Verification
  - → Sometimes Extra HW Needed

Limited HW-SW Interaction

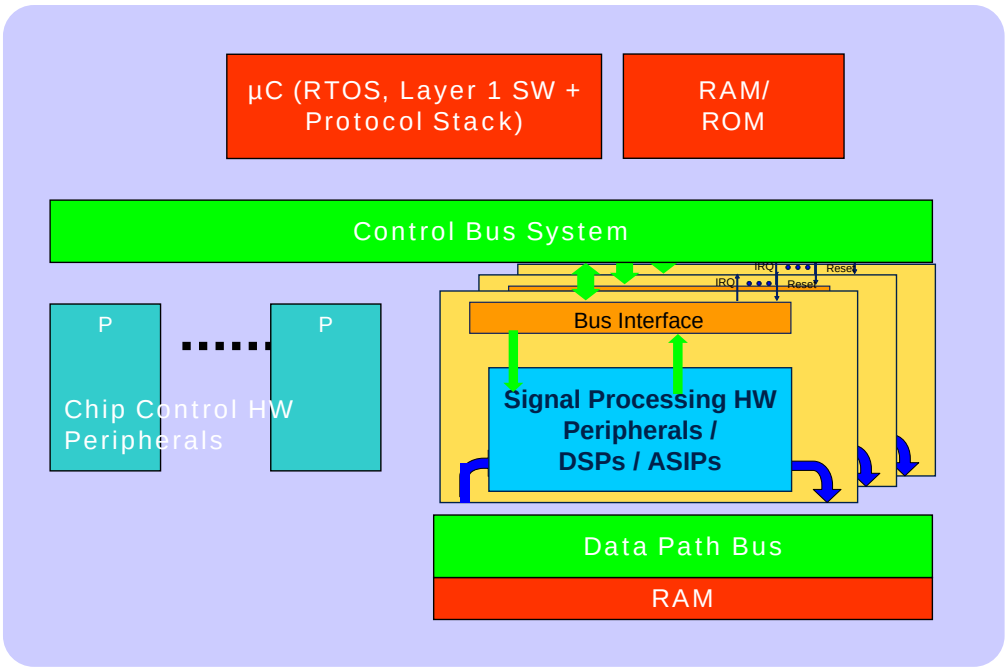
- HW-SW Split: Encapsulate Functionality in HW
  - → HW-SW Interface Natural Boundary for Function Clusters
  - → Latency Critical Paths in HW
  - → Simplified SW Scheduling
  - → No Critical HW-SW Interactions
- Configuration Granularity: UMTS Slot (667 µs) and Frame (10 ms) Boundaries
  - → Simplified Verification

Performance vs Complexity

Flexibility Where Needed

- Algorithm Design:
  Robust and "As Good As Needed"

Digital Baseband Detailed Architecture

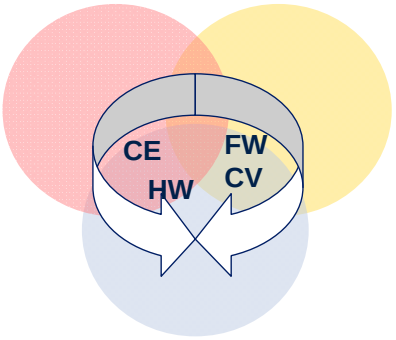


Separate functionality into autonomous subsystems

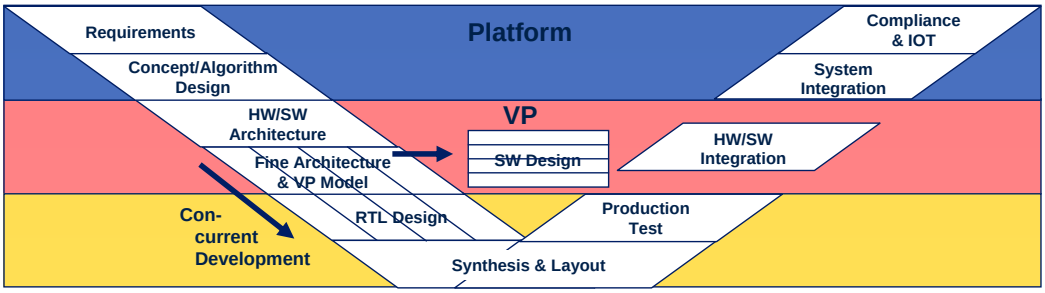
System Architecture Concept

"System View" Required (Cross-Layer, -Functional, -Disciplinary)

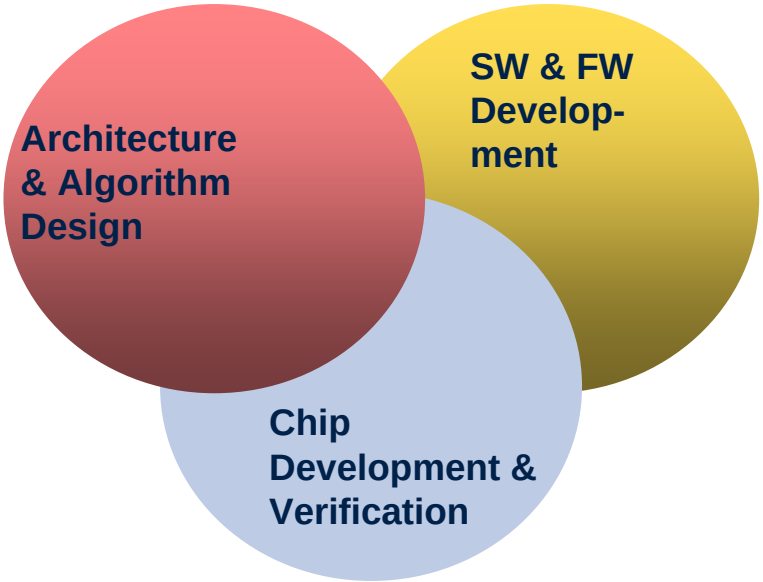
- split up development in parallel streams
  - one team for each HW-Processing element
  - cross-functional setup



- system level oriented flow for each sub-component:



Team & Project Setup



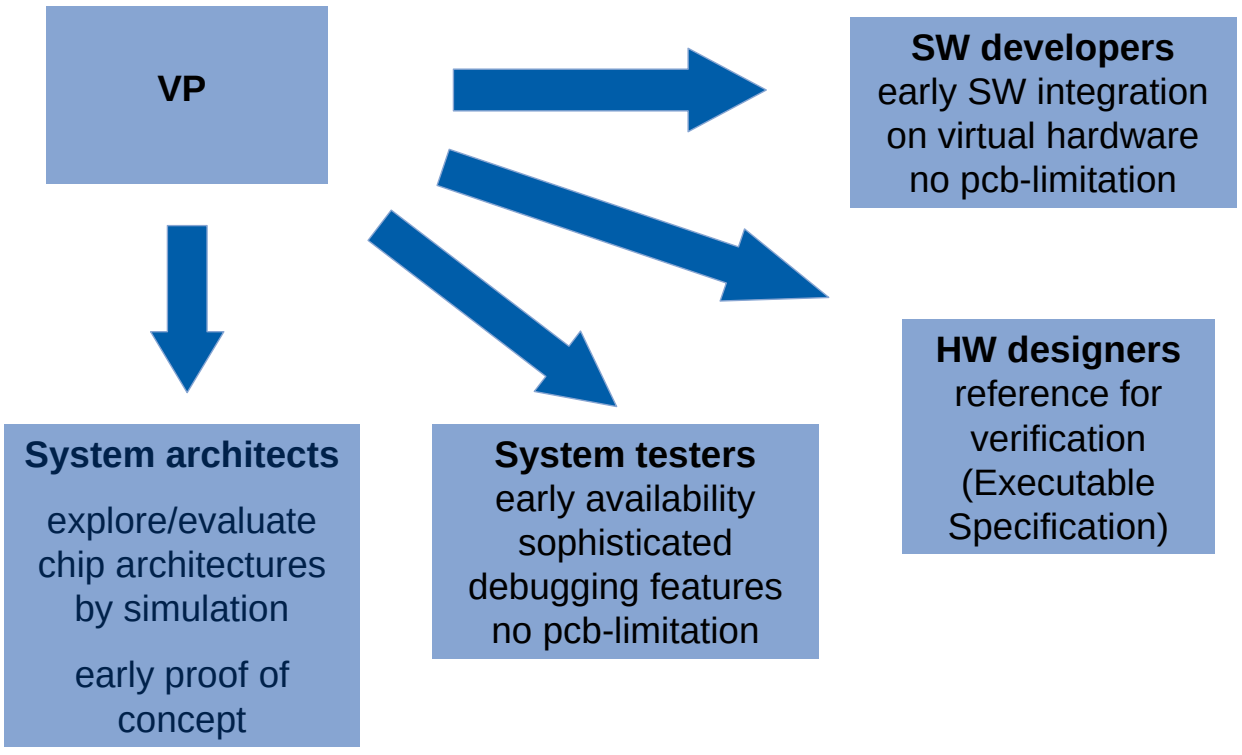
interdisciplinary teams:
- Concept & Algorithms
- HW development
- SW development
- System verification

joint responsibility

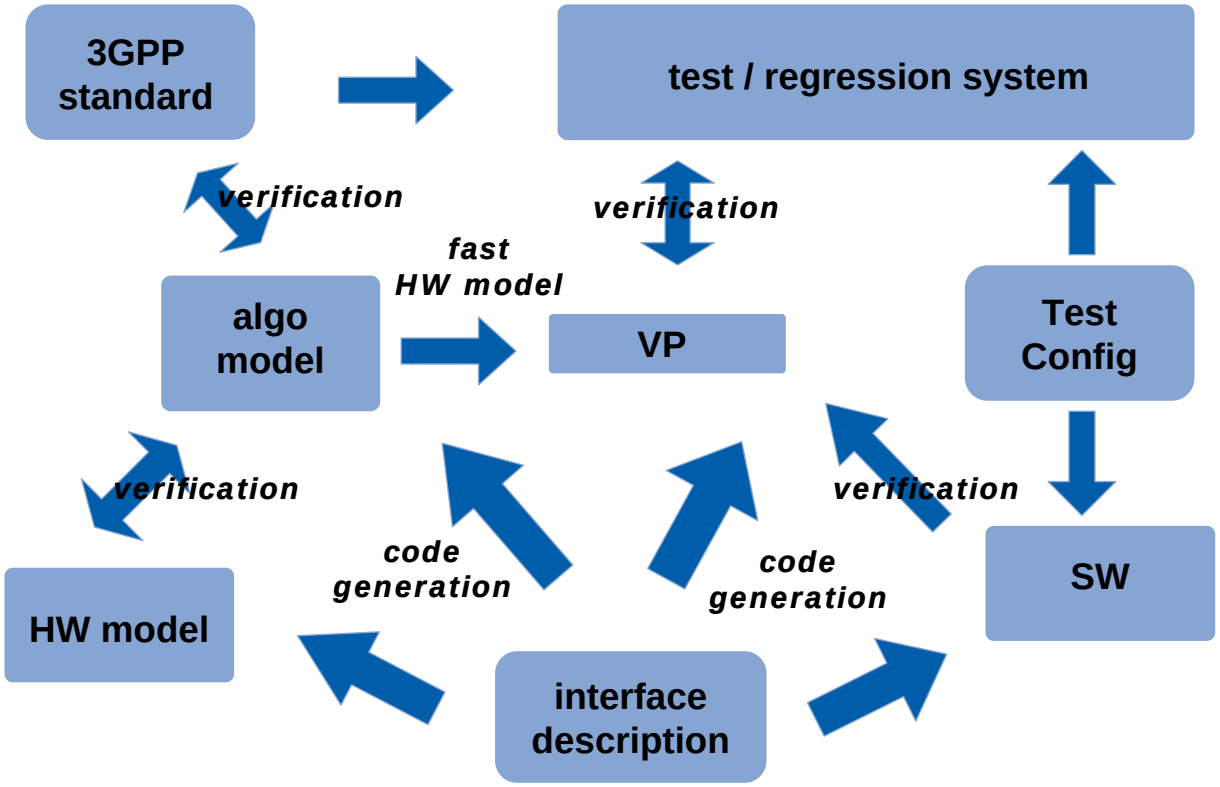
- Block level design & verif.
- Architecture refinement
- HW/FW codesign
- System integration

Methodology

Key Methodology: Virtual Prototype

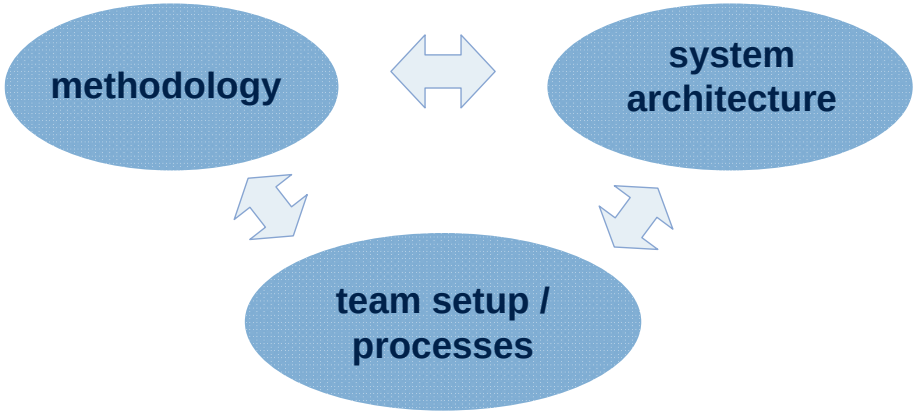


Methodology: Bridging Levels of Abstraction



Methodology

- VP is *the* essential vehicle for system integration and verification
- Integrated tool landscape to provide maximum reuse
- Seamless transition between different levels of abstraction
- Platform for cross-functional team interaction
- Provide uniform touch-and-feel throughout all project phases



Conclusion

- Wireless SoC design is one of the biggest challenges in the industry
- Greatest challenge:
  - System reconfigurability
  - Latency critical loops
  - *Not* data-throughput
- Success requires a system-level approach:
  - Exhaustive and detailed system knowledge
  - Interdisciplinary teams
  - Integrated design and verification flow